WE CLAIM:

1. An apparatus for adjusting a pulse width of a control signal, comprising:

a first comparator circuit that is arranged to provide a start signal in response to a ramp signal and a ramp reference level;

a second comparator circuit that is arranged to provide a stop signal in response to a feedback signal and the ramp signal, wherein the feedback signal is related to the pulse width of the control signal;

a first memory circuit that is arranged to provide a memory clock signal such that the memory clock signal is: asserted in response to the start signal and de-asserted in response to a clock signal;

a second memory circuit that is arranged to adjust the control signal such that the control signal is: de-asserted when a reset signal is asserted, and asserted in response to the memory clock signal when the reset signal is de-asserted;

a logic circuit that is arranged to adjust the reset signal such that the reset signal is asserted when the start and stop signals are both asserted; and

a feedback circuit that is arranged to provide the feedback signal, wherein the feedback signal is related to the control signal.

2. The apparatus of Claim 1, wherein the first comparator circuit has a built-in offset that has a dominant effect on the pulse width.

3. The apparatus of Claim 1, wherein the ramp reference level corresponds to at least one of: a minimum level associated with the ramp signal, and a sum of the minimum level associated with the ramp signal and an offset amount such that the ramp reference level has a dominant effect on the pulse width.

4. The apparatus of Claim 1, wherein the first comparator circuit includes an unbalanced differential pair such that the first comparator has a built-in offset with a predictable polarity and a predictable minimum magnitude.

5. The apparatus of Claim 1, wherein the second comparator circuit is a rail-to-rail comparator.

6. The apparatus of Claim 1, wherein the second comparator includes a p-type differential pair and an n-type differential pair that are arranged to operate with a rail-to-rail common-mode input range.

7. The apparatus of Claim 1, wherein the first memory circuit comprises an SR-type latch.

8. The apparatus of Claim 1, wherein the second memory circuit comprises a D-type flip-flop.

9. The apparatus of Claim 1, wherein the logic circuit is also arranged to assert the reset signal in response to at least one of: the assertion of the clock signal, and the assertion of a power-on-reset signal.

10. The apparatus of Claim 1, further comprising an output circuit that is responsive to the control signal such that the apparatus is operated as a switching converter.

11. The apparatus of Claim 1, further comprising an output circuit that is arranged to provide an output voltage in response to the control signal such that the magnitude of the output voltage is related to the pulse width of the control signal.

12. The apparatus of Claim 11, wherein the feedback circuit is arranged to sense the output voltage to provide the feedback signal.

13. The apparatus of Claim 11, wherein the feedback circuit includes an error amplifier that is responsive to the output voltage to provide the feedback signal.

14. The apparatus of Claim 1, wherein the ramp signal is initiated in response to the clock signal.

15. An apparatus that is arranged to monitor an output voltage to adjust a pulse width that is associated with a pulse control signal, the apparatus comprising:

a feedback means that is arranged to provide a feedback signal that is responsive to the output voltage;

a ramp means that is arranged to initiate a ramp signal in response to a clock signal;

a first comparator means that is arranged to provide a start signal in response to the ramp signal and a ramp reference level;

a second comparator means that is arranged to provide a stop signal in response to the feedback signal and the ramp signal;

a first memory means that is arranged to provide a memory clock signal in response to the start signal and a clock signal; and

a second memory means that is arranged to deactivate the pulse control signal when the start signal and the stop signal are both asserted, and also arranged to activate the pulse control signal when the memory clock signal has an edge transition.

16. The apparatus of Claim 15, wherein the first comparator means has a built-in offset that has a dominant effect on the pulse width.

17. The apparatus of Claim 15, wherein the ramp reference level corresponds to at least one of: a minimum level associated with the ramp signal, and a sum of the minimum level associated with the ramp signal and an offset amount such that the ramp reference level has a dominant effect on the pulse width.

18. The apparatus of Claim 15, wherein the apparatus is arranged such that a pulse width associated with the pulse control signal linearly ranges down to an approximate value of zero.

19. The apparatus of Claim 15, further comprising an output means that is arranged to provide the output voltage in response to the pulse control signal.

20. A method for adjusting a pulse width that is associated with a pulse control signal, the apparatus comprising:

monitoring an output voltage;

providing a feedback signal in response to the output voltage;

initiating a ramp signal in response to a clock signal;

comparing the ramp signal to a reference signal;

asserting a start signal when the ramp signal exceeds the reference signal;

comparing the ramp signal to the feedback signal;

asserting a stop signal when the ramp signal exceeds the feedback signal;

de-asserting the pulse control signal when the stop signal and the start signal are asserted; and

asserting the pulse control signal when the start signal is asserted and the stop signal is de-asserted.